REMARKS

Claims 1-29 were examined and reported in the Office Action. Claims 1-9 and 18-29 are rejected. Claim 4 is canceled. Claims 1-2, 4-8, 10, 13, 18-19 and 23-25 are amended. Applicant confirms the elected claims are claims 1-9 and 18-29, which were elected with traverse. Claims 1-3 and 5-29 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. In the Drawings

The drawings are objected to due to minor informalities.

Applicant has amended Figures 4, 7A, 7B, 8A, and 8B. Replacement sheets are submitted herewith. Approval is respectfully requested.

II. 35 U.S.C. §101, Second Paragraph

It is asserted in the Office Action that claims 18-23 are rejected under 35 U.S.C. §101, because the claimed invention is directed to non-statutory subject matter. Applicant has amended the specification to remove the disclosure regarding carrier waves. Applicant has no intent to claim the limitations of carrier waves.

Accordingly, withdrawal of the 35 U.S.C. §101 rejections for claims 18-23 are respectfully requested.

III. 35 U.S.C. §112, first and second paragraphs

A. It is asserted in the Office Action that claims 4, 18 and 24 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Applicant has amended the claims with the limitations of adding debug fields to the control status register *field*. It is well known in the art that fields can be added/attached to other fields within a register.

Accordingly, withdrawal of the 35 U.S.C. §112, first paragraph rejections for claims 4, 18 and 24 are respectfully requested.

B. It is asserted in the Office Action that claims 2-3, 7-8, 19 and 23-29 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has amended claims 2, 7, 19, 23, 24 and 25 to overcome the 35 U.S.C. §112, second paragraph rejections.

Accordingly, withdrawal of the 35 U.S.C. §112, second paragraph rejections for claims 2-3, 7-8, 19 and 23-29 are respectfully requested.

IV. 35 U.S.C. § 102(b)

It is asserted in the Office Action that claim 1-3 and 9 is rejected under 35 U.S.C. § 102(b), as being anticipated by U. S. Patent No. 5,694,589 issued to Glew et al. ("Glew"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2131,

> '[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)).

Glew discloses using debug registers where addresses of breakpoints are stored (Glew, col. 4, lines 33-49). Glew does not teach, disclose or suggest Applicant's amended claim 1 limitations of "said controller adds at least three debug register bit fields to at least one processor control status register field, wherein said at least three register bit fields comprise a run field, a single step field and a debug enable field."

Therefore, since Glew does not teach, disclose or suggest all of Applicant's amended claim 1 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. §

102(b) has not been adequately set forth relative to Glew. Thus, Applicant's amended claim 1 is not anticipated by Glew.

Accordingly, withdrawal of the 35 U.S.C. § 102(b) rejections for claims 1-3 and 9 are respectfully requested.

V. 35 U.S.C. § 103(a)

A. It is asserted in the Office Action that claims 4-6, 18-22 and 24-28 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over Glew in view of U. S. Patent No. 6,951,416 issued to Deng et al. ("Deng"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2142

> [t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." "*All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's claims 5-6 (claim 4 being canceled) directly depend on amended claim 1. Applicant has addressed Glew above in section V regarding amended claim 1.

Applicant's amended claim 18 includes the limitations of "adding at least one breakpoint bit field directly to each of a plurality of instructions, adding at least three debug register bit fields directly to at least one processor control status register field."

Applicant's amended claim 24 includes the limitations of "adding at least one breakpoint bit field directly to each of a plurality of instructions, adding at least three breakpoint register bit fields to at least one processor control status register field, wherein the attached at least one breakpoint bit field is an additional field directly added to each processor instruction."

Deng discloses a breakpoint control register (see Deng, Fig. 16, col. 9, lines 21-26). Deng, however, does not teach that a "said controller adds at least three debug register bit fields to at least one processor control status register field, wherein said at least three register bit fields comprise a run field, a single step field and a debug enable field." That is, the processor control status register already exists with a predefined field structure. Applicant's claimed invention makes use of this preexisting structure and changes the field structure by adding at least three debug register fields. The processor control status register is not a breakpoint control register.

Therefore, even if the teachings of Glew are combined with Deng, the resulting invention would still not teach, disclose or suggest Applicant's amended claim 1 limitations of "the controller to execute a debug process, said debug process attaches at least one breakpoint bit field directly to each of a plurality of processor instructions, wherein said controller adds at least three debug register bit fields to at least one processor control status register field, wherein said at least three register bit fields comprise a run field, a single step field and a debug enable field," Applicant's amended claim 18 limitations of "adding at least one breakpoint bit field directly to each of a plurality of instructions, adding at least three debug register bit fields directly to at least one processor control status register field," nor Applicant's amended claim 24 limitations of "adding at least one breakpoint bit field directly to each of a plurality of instructions, adding at least three breakpoint register bit fields to at least one processor control status register field, wherein the attached at least one breakpoint bit field is an additional field directly added to each processor instruction."

Since neither Glew, Deng, and therefore, nor the combination of the two, teach, disclose or suggest all the limitations of Applicant's amended claims 1, 18 and 24, as listed above, Applicant's amended claims 1, 18 and 24 are not obvious over Glew in view of Deng since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claims 1, 18 and 24, namely claims 5-6, 19-22, and 25-28, respectively, would also not be obvious over Glew in view of Deng for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 4-6, 18-22, 24-28 are respectfully requested.

B. It is asserted in the Office Action that claims 7-8, 23 and 29 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over Glew.

Applicant's claims 7-8 either directly or indirectly depend on amended claim 1. Applicant has addressed Glew above in section IV regarding amended claim 1. Applicant's claim 23 directly depends on amended claim 18. Applicant has addressed Glew above in section V(A) regarding amended claim 18. Applicant's claim 29 directly depends on amended claim 24. Applicant has addressed Glew above in section V(A) regarding amended claim 24.

Glew does not teach, disclose or suggest Applicant's amended claim 1 limitations of "the controller to execute a debug process, said debug process attaches at least one breakpoint bit field directly to each of a plurality of processor instructions, wherein said controller adds at least three debug register bit fields to at least one processor control status register field, wherein said at least three register bit fields comprise a run field, a single step field and a debug enable field," Applicant's amended claim 18 limitations of "adding at least one breakpoint bit field directly to each of a plurality of instructions, adding at least three debug register bit fields directly to at least one processor control status register field," nor Applicant's amended claim 24 limitations of "adding at least one breakpoint bit field directly to each of a plurality of instructions, adding at least three breakpoint register bit fields to at least one processor control status register field, wherein the attached at least one breakpoint bit field is an additional field directly added to each processor instruction."

Since Glew does not teach, disclose or suggest all the limitations of Applicant's amended claims 1, 18 and 24, as listed above, Applicant's amended claims 1, 18 and 24 are not obvious over Glew in view of no other prior art since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claims 1, 18 and 24, namely claims 7-8, 23, and 29, respectively, would also not be obvious over Glew in view of no other prior art for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 7-8, 23 and 29 are respectfully requested.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-3 and 5-29 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: August 13, 2007

By: _____
Steven Laut, Reg. No. 47,736

1279 Oakmead Parkway
Sunnyvale, California 94085-4040
(310) 207-3800

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

_____
Jean Svoboda Date: August 13, 2007